APPLICATION FOR UNITED STATES LETTERS PATENT

FOR

TEST ACCESS PORT

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TEST ACCESS PORT

BACKGROUND

1.   Field

5   This disclosure relates to the testing of multi-core processors.

2.   Background Information

A Test Access Port (TAP) typically comprises a 4 or 5-pin serial test interface that is compliant with the IEEE 1149.1 specification. *IEEE Standard Test Access Port*

10   *and Boundary-Scan Architecture*, IEEE Std 1149.1a-1993. It may be used as an access mechanism to implement a boundary scan architecture, as well as other test modes employed to implement the Design For Testability (DFT) methodology on a given integrated circuit (IC). Traditional microprocessor designs have employed a TAP as a mechanism for testing.

15   A TAP typically has multiple uses. For example, when testing a chip, it is used in a test and manufacturing environment to help debug the chip. As another example, in a system environment, a TAP is used to perform board level interconnect testing between two or more board level components.

As the trend towards higher integration on a given piece of silicon continues, a

20   new class of microprocessors, multi-core microprocessors, have appeared. Traditional microprocessors typically include a block of circuitry which substantially includes the core functions of the processor (hereafter, the "processor core") and one or more circuit blocks which substantially contain non-core functions, such as, for example, comprising

cache, front side bus logic, pads, *etc.* (hereafter, the "non-processor core" or "non-core").

In contrast, multi-core processors may contain or include a plurality of processor cores

and one or more non-processor cores.

Typically, the processor core houses a TAP for the processor. By substantially

5   duplicating the processor core on the integrated circuit (IC), the number of TAPs will,

therefore, be increased in this situation. This would potentially increase the number of

pins for the IC package. In addition, there may potentially be increases in test time and

test vector depth, in order to test each processor core independently. A need, therefore,

exists for an improved apparatus or method for implementing an IEEE 1149.1 compliant

10   test access port for a multi-core IC processor.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter regarded as the invention is particularly pointed out and

distinctly claimed in the concluding portions of the specification. The invention,

15   however, both as to organization and the method of operation, together with objects,

features and advantages thereof, may be best understood by a reference to the following

detailed description when read with the accompanying drawings in which:

FIG. 1 is a diagram illustrating an embodiment of a test access port (TAP) in

accordance with the invention;

20   FIG. 2 is a diagram illustrating a typical configuration of a test access port (TAP)

in a multiple processor configuration.

FIG. 3 is a four-part diagram illustrating an embodiment of multiple couplings of

a test access port (TAP) in accordance with the invention.

FIG. 4 is a four-part diagram illustrating an embodiment of a test access port (TAP) in accordance with the invention.

FIG. 5 is a diagram illustrating a distributed test access port (TAP) mechanism in a single core processor.

5   FIG. 6 is a diagram illustrating an integrated test bus (ITB) in accordance with the invention.

FIG. 7 is a diagram illustrating an embodiment of a TAP Core Configuration Register in accordance with the invention.

FIG. 8 is a state diagram illustrating an embodiment of a test access port (TAP)

10   finite-state machine (FSM) in accordance with the IEEE 1149.1 specification.

FIG. 9 is a diagram illustrating an embodiment of a test access port (TAP) data register in accordance with the IEEE 1149.1 specification.

DETAILED DESCRIPTION

15   In the following detailed description, numerous details are set forth in order to provide a thorough understanding of the present invention. However, it will be understood by those skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as to not obscure the present invention.

20   To provide a context for the invention, a Test Access Port (TAP) typically comprises a 4 or 5-pin serial test interface that is compliant with the IEEE 1149.1 specification. It may be used as an access mechanism to implement the boundary scan architecture, as well as other test modes typically employed to implement the Design For

Testability (DFT) methodology on a given integrated circuit. Traditionally, microprocessor designs have employed a TAP as a mechanism for testing.

A TAP, in accordance with the IEEE 1149.1 specification, is employed by a large number of integrated chip designers and manufacturers. One of the purposes of a TAP is

5   to facilitate testing of an integrated circuit. For example, a board manufacturer, attempting to verify that their board's components are properly coupled, may couple a number of the board's integrated chips' TAPS into a serial chain and shift data through that chain. This procedure is frequently referred to as 'boundary-scan', because data is scanned across the pin boundary of the board's integrated chips.

10   In another example, an integrated circuit designer may, as an example, wish to adjust the speed of the circuit's clock during specific logic stages. While the IEEE 1149.1 specification does not contain a specification regarding this form of testing, in order for the integrated circuit designer to accomplish this, one may, as one of many possible design choices, leverage the TAP specification to allow access to this test

15   feature. Instructions substantially regulating the speed and timing of the clock may be scanned or shifted into the integrated circuit via the TAP. An integrated circuit designer may leverage a test access port that is substantially IEEE 1149.1 compliant to facilitate a variety of testing features, of which the above is merely one possible example.

The IEEE 1149.1 standard specifies a possible 4 pin interface which may be

20   utilized to allow test instructions and associated test data to be fed into a component and, subsequently, may allow the results of execution of such instructions to be read out of the component. For testing features enumerated in the IEEE 1149.1 specification, information is communicated in a serial format. However, additional testing features that

utilize a test access port, which is substantially IEEE 1149.1 compliant, may not be restricted in this fashion.

An IEEE 1149.1 compliant test access port includes the following 4-pin interface:

- Test Clock (TCLK) acts as the clock signal for the test access port;

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- Test Mode Select (TMS) controls the TAP Finite-State Machine (FSM); The TMS pin may be sampled by the FSM every TCLK and is utilized in the determination of whether to or how to change or retain the state of the FSM;

- Test Data In (TDI) provides the input of serial movement of test data

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through the circuit;

- Test Data Out (TDO) provides the output of serial movement of test data through the circuit.

The IEEE 1149.1 standard details an optional, but frequently implemented, fifth interface pin, Test-Logic-Reset (TLR). The TLR pin may be used to reset the TAP's FSM to a

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known state.

A Test Access Port Controller (TAPC) usually controls the interaction between the TAP's 4-pin serial interface and the circuit's testing features. A TAPC may control this interaction based on the current state of a TAP's 16-state FSM and the active instruction in the TAP's Instruction Register. FIG. 8 shows a TAP FSM as detailed in

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section 5.1, TAP Controller State Diagram, of the IEEE 1149.1 specification. Such a FSM may be conceptually divided into 3 main parts. State grouping 801 allows access to the TAP's Instruction Register. State grouping 802 allows access to the variety of data and control registers possibly utilized in the implementation of any test features

accessible by the circuit's TAP. State grouping 803 includes a state which may reset the TAP to a known state and a state which may, depending on the test feature's implementation, place the TAP in an idle state.

In addition to the state of the FSM, access to a TAP's data and control registers is

5   conditioned on the active instruction in the TAP's Instruction Register. The Instruction Register (IR) may be accessed when the TAP FSM is placed in one of the states in state grouping 801. In state grouping 801 an instruction may be shifted into the Instruction Register. In an IEEE 1149.1 compliant TAP, an instruction usually places one data or control register serially between the TDI and TDO pins. A single register may be

10   selected by multiple instructions depending on the design of the IC's particular TAP.

Generally, but not always, a TAP's data and control registers contain both a serial and parallel component, as seen in FIG. 9. However, a register may deviate from this norm in order to accomplish specific testing or implementation goals as the designers see fit. Once an instruction, that activates a particular register, has been shifted into the TAP,

15   the register may be affected by the TAP FSM states in grouping 802.

Below is an illustrative example of a basic access of a data or control register. However, due to special testing or implementation goals, a TAP may incorporate additional actions that may or may not occur during the operation of a TAP. The following is merely one possible example, of the operation of a sample TAP and is not

20   intended to limit the scope of the invention or to represent the operation of all TAPs included within the scope of the present invention.

When in the CAPTURE-DR state, an active register may normally load, in a parallel method, the contents of its parallel component into its serial component. It is

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normally said that the parallel component is being "read" or "captured." When in the SHIFT-DR state, an active register may serially shift data from TDI to TDO across its serial component. During this time, the parallel register will generally not be affected. When in the UPDATE-DR state, an active register may normally load, in a parallel

5   fashion, the contents of its serial component into its parallel component. It is normally said that the parallel component is being "written to" or "updated."

The IEEE 1149.1 specification details the base level of functionality for a TAP, however, integrated chip (IC) designers frequently add additional functionality to a TAP. This additional functionality may, for example, address certain testing aspects of the IC,

10   be hidden from the customer or board manufacturer, allow access to non-test related functions of the IC, *etc.*

Typically, the TAPC and the plurality of data and control registers are placed together in a particular location on the IC. However, some registers, for example those dealing with scan testing, are dispersed throughout the chip. In addition, it may be

15   desirable for the TAPC to communicate with other functional units blocks (FUBs) on the IC, *e.g.* floating-point unit, instruction fetch unit, memory, *etc.* This dispersion may at times create a large number of control signals, which may radiate from the TAPC to the dispersed registers. Because ICs have a limited amount of space for routing signals, dedicating a large portion of this routing space to testing, instead of core functionality,

20   may result in routing and other problems during chip design and manufacture.

FIG. 5 is a diagram illustrating a distributed test access port mechanism implemented in a single-core processor. The Integrated TAP Controller (ITC) 510, which may include the TAPC and some data and control registers, may be coupled to

distributed registers, such as, for example, 530-533, and/or FUBs 521 & 522 via Integrated Test Bus (ITB) 550, for example. ITB 550 may comprise a grouping of data signals that allow the receiving registers and/or FUBs to locally generate control signals desired for operation, as opposed to generating the control signals directly from the

5   TAPC.

FIG. 6 illustrates a possible grouping of data signals that may achieve this goal. Bit 0 of ITB 550 may be a representation of the current TDI bit. Bits 1-4 may be a representation of the state of the TAP FSM. Bits 5-10 may be a representation of the active contents of the TAPC's Instruction Register, assuming the Instruction Register is

10   6-bits wide, however any Instruction Register width may be used. In addition, other bits may be added to ITB 550 as desired to provide information for the distributed registers 530-533 and/or FUBs 521 & 522 in order to locally generate the control signals for operation. Also, the order of the bits may vary depending, at least in part, on the embodiment of the ITB.

15   As the trend towards higher integration on a given piece of silicon continues, a new class of microprocessors, multi-core microprocessors, have appeared. Conventional microprocessors typically include a block of circuitry which substantially includes the core functions of the processor (hereafter, the "processor core") and one or more circuit blocks which substantially include non-core functions, possibly comprising cache, front

20   side bus logic, pads, *etc.* (hereafter, the "non-processor core" or "non-core"). In contrast, multi-core processors may include a plurality of processor cores and one or more non-processor cores.

Typically, the processor core houses the TAP controller of the processor. Substantially duplicating the processor core on the integrated circuit (IC) will, therefore, increase the number of TAP controllers. This, increase in the number of processor cores, may potentially increase the number of pins employed on the IC package, as well as

5   potentially increase the test time and the test vector depth utilized to test multiple processor cores. In addition, if it is desired that a multi-core processor be a "plug-in" replacement for a single-core processor, the pin out of the multi-core processor should substantially match the pin-out of the single-core processor. Therefore, the number of pins for TAP access on a multi-core processor may be limited to the number of pins on

10   the single-core processor. A need, therefore, exists for an improved apparatus or method for implementing an IEEE 1149.1 compliant test access port for a multi-core processor.

A technique for providing a improved IEEE 1149.1 compliant test access port for a multi-core processor may include: providing a TAPC on at least two processor cores, providing a TAP configuration register in the non-processor core, coupling the multiple

15   core TAPCs and the non-processor core configuration register such that one of multiple routing and control configurations may be dynamically selected during operation. Such a device may reduce the number of pins employed on the IC package, and provide opportunities for reducing the number of testing vectors and time utilized to test the multi-core device. In addition, such a device may allow a multi-core processor to be

20   "plug-in" compatible with a single-core processor.

In light of the above illustrative context for the invention, it may be understood that FIG. 1 is a block diagram illustrating an embodiment of a multi-core processor in accordance with the invention. Embodiment 100 includes processor cores 110 & 120,

although any number of processor cores may be used, and non-processor core 130, although any number of non-processor cores may be used. Both processor cores 110 & 120 may include TAPCs 111 & 121.

In the embodiment illustrated in FIG 1, both TAPCs may receive identical or

5   substantially identical TLR, TMS, and TCLK signals via bus 150. However, the invention is not limited to embodiments where all TAPCs receive identical or substantially identical TLR, TMS and TCLK signals. The TAPCs may receive fully or partially independent TLR, TMS and TCLK signals. In addition, because the TLR signal is optional under the IEEE 1149.1 specification, some or all of the TAPCs may not

10   receive the TLR signal. These fully or partially independent signals may each have fully or partially independent external IC pin interfaces or a particular routing technique may be used internally to the IC. For example, a routing scheme similar to that used in the embodiment illustrated in FIG 1 for the TDI and TDO signals, described below, may be employed in order to provide fully or partially independent TLR, TMS and TCLK

15   signals. However, the invention is not limited to any particular routing scheme for these signals.

Both TAPCs 110 & 120 may produce their own TDO signals 113 & 123, which may be routed in accordance with one of many selectable configurations by TAP Control Switch 139. TAP Control Switch 139 provides a single TDO to external TDO signal

20   153. External TDI signal 152 may be routed in accordance with one of many selectable configurations by TAP Control Switch 139. TAP Control Switch 139 provides TAPCs 111 & 121 with independent TDIs 112 & 122. TAP Control Switch 139 may route the TDI/TDO signals using multiplexer (MUX) or demultiplexer (DeMUX) components,

however, one skilled in the art will instantly recognize that a variety of electrical components may be used to perform the desired routing operation.

TAP Control Switch 139 may be controlled by TAP Core Configuration Register 135. TAP Core Configuration Register 135 may be readable and writeable by, as taught

5   by the IEEE 1149.1 specification, serially shifting data into and out of the register with the entering bit being TDI and the exiting bit being Register TDO 133. However, a variety of access mechanisms, either compliant or non- compliant with the IEEE 1149.1 specification, may be employed in order to read and/or write to Register 135. In this embodiment, TAP Core Configuration Control Logic 138 may receive ITBs 114 & 124,

10 one from each TAPC. Alternately, in another possible embodiment, TAP Core Configuration Control Logic 138 may receive control signals that are more detailed and specialized than the generic signals employed in ITBs 114 & 124. MUX 136 may determine which processor core has control of non-processor core 130 and supplies TAP Core Configuration Control Logic 138 with the controlling ITB, ITB 134. Of course, any

15 grouping of components, instead of MUX 136, may be used to perform the desired routing operation.

If multiple data and control registers are employed in the non-processor core, in accordance with the IEEE 1149.1 specification, each register will provide a TDO to the TAPCs. It may be desirable to reduce the number of TDOs returned to TAPCs 111 &

20 121 from the non-processor core. MUX 137 may be utilized to select which of the multiple TDOs is to be returned from non-processor core 130 to TAPCs 111 & 121. Of course, any grouping of components, instead of MUX 137, may be used to perform the desired reduction operation. While the embodiment in FIG. 1 utilizes this TDO reduction

the invention is not limited by supplying any particular number of TDO signals from non-processor core 130. The invention is also not limited to having only one non-processor core.

5 In the embodiment of the invention illustrated in FIG. 7, TAP Core Configuration Register 135 includes a bit to determine which processor-core's TAPC is allowed to control the non-processor core data and control registers, of which one is the TAP Core Configuration Register itself. Although the embodiment in FIG.1 illustrates two processor cores, the invention is not limited to embodiments with two processor cores. More bits may be used for embodiments with more than two processor cores. By default, 10 this bit may be set to a substantially predetermined value. The substantially predetermined value may be loaded into the register upon a predetermined event such as, but not limited to: the IC receiving the "Power Good" signal from the power supply, activation of the IC's master reset pin, activation of the IC's TLR pin, or one or more of many other possible events. This bit may be used in conjunction with MUX 136 to 15 determine which ITB the non-processor core will use as ITB 134.

In the embodiment of the invention illustrated in FIG. 7, TAP Core Configuration Register 135 includes a number of bits to determine the routing of the processor cores' TDI and TDO signals. Possible embodiments of routing configurations are illustrated in FIGs. 3 and 4. These routing configurations may be contrasted with the traditional 20 routing configuration used for multiple processor systems, as illustrated by FIG. 2. In a multiple processor system two or more processors, each processor including a processor-core and a non-processor core, are utilized. In traditional multi-processor TAP routing, processors 210 & 220 may receive substantially identical TLR, TMS, and TCLK signals

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via bus 250. Processor 210 may receive its TDI signal from the external TDI signal 252.

Processor 210's TDO 212 may be daisy-chained via signal 260 to processor 220's TDI

223. Processor 220 then supplies its TDO signal to the external TDO signal 253. This

allows one to shift data into either processor's TAPC. However the serial data chain,

5   TDI 252 to TDO 253, is now effectively double that of a single processor's serial data

chain. By doubling the effective length of a processor's serial data chain the amount of

time to test the processor is effectively doubled.

In the embodiment of the invention illustrated in FIG.1, TAP Core Configuration

Register 135 includes a number of bits to determine the routing of the processor cores'

10   TDI and TDO signals. These bits may control which routing configuration of TAP

Control Switch 139 is selected. One skilled in the art may realize a number of ways to

implement the TAP Control Switch 139. For example, MUXs may be used, however the

invention is certainly not limited to this embodiment of TAP Control Switch 139, and all

are included within the scope of the present invention. Particular embodiments of these

15   routing schemes are illustrated in FIGs 3 & 4. However, the invention is not limited to

these illustrated routing schemes. The routing of external TDI 152 to external TDO 153

may involve routing the signals to the controlling TAPC's, as determined by TAP Core

Configuration Register 135, the TDI/TDO signals. This may allow the multi-core

processor to be accessed as if the controlling processor core existed within the IC. The

20   non-controlling TAPC's TDI and TDO signals may be either disconnected or set to a

substantially predetermined value. FIGs 3a & 3b illustrate embodiments where external

TDI 152 and external TDO 153 are routed directly to the TDI and TDO signals of the

controlling processor-core's TAPC. FIG 3a illustrates an example where processor-core

120's TAPC 111 is the controlling TAPC. FIG. 3b illustrates an example where processor-core 120's TAPC 121 is the controlling TAPC.

In the embodiments of the invention illustrated in FIGs 3c and FIG 3d, the ability to serially daisy-chain the processor-cores' TAPs is shown. TAP Core Configuration
5 Register 135 may be used to control the order of the processor-cores in the serial daisy-chain. FIG. 3c illustrates a routing scheme where processor-core 110 may be first in the chain and processor-core 120 last in the chain. FIG. 3d illustrates a routing scheme where the order of the processor-cores in the serial chain is reversed from that illustrated in FIG. 3c. The order of the processor-cores in the daisy chain may be determined with
10 the aid of the control bit found in TAP Core Configuration Register 135 or the order may be determined without reference to this bit.

In contrast to FIGs 3c & 3d, where the processor-core's serial data chains may be accessed in a serial fashion, FIG. 4 illustrates a possible routing configuration where the processor-core's serial data chains may be accessed in parallel. Once again, TAP Core
15 Configuration Register 135 may control which of these routing configurations of TAP Control Switch 139 are selected. In this particular routing configuration, external TDI 152 is applied to the TDI signals of each processor-core's TAPC. If only one external TDO pin exists, the controlling TAPC's TDO signal may be placed on external TDO 153. FIG. 4a illustrates an embodiment where processor-core 110 is selected as the controlling
20 TAPC and its TDO signal is placed on external TDO 153. FIG. 4b illustrates the case where processor-core 120 is selected as the controlling TAPC.

Although in these embodiments the processor-cores are substantially identical, the invention is not limited to embodiments with identical processor-cores. It may be useful

to test the processor-cores in parallel and determine if the testing results are not substantially identical. To aid in this, a comparison mechanism may be used. FIG. 4 illustrates embodiments with this comparison mechanism. In FIG. 4a, exclusive OR (XOR) gate 440 compares the TDO signals from processor-cores 110 & 120. When the

5   two TDO signals are not substantially identical, XOR gate 440 may signal that a mis-compare has occurred. Depending on which routing is selected by TAP Control Switch 139, this mis-compare signal or "error bit" may be stored in a register, placed on external TDO signal 153 or both. In an embodiment, illustrated in FIGs. 4c and 4d, where the mis-compare bit is placed onto external TDO signal 153, external TDO signal 153 may

10   be allowed to freely change between high and low states, as determined by the state of the mis-compare bit, or may be designed to get "stuck" in a particular state once a mis-compare has occurred, referred to as a "sticky-bit." In an embodiment where the mis-compare signal is stored in a register, the embodiment may involve storing the signal in a sticky-bit register, although other storage schemes are possible. This register may then

15   be accessed via the TAP or possibly though the processor's normal register access techniques. However, the invention is not limited to the technique used to access the register.

It is noted that, while FIGs. 1, 3 & 4 illustrate embodiments with two identical processor-cores and a single non-processor core, the invention is not limited to this

20   embodiment. It is recognized that as the number of processor cores increases beyond two, the number of possible routing configurations that may be provided by TAP Control Switch 139 also increases. While the embodiments shown illustrate configurations where the processor-cores are accessed in exclusively independent, serial or parallel modes, as

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the number of processor cores increases, routing configurations that include a mix of the independent, serial and parallel modes are possible. In addition, as the number of non-processor cores increases, more routing schemes may be available. If substantially non-identical processor-cores are used, additional routing schemes may exist or illustrated

5 routing schemes may no longer be desirable. The invention is not limited to a particular defined set of routing configurations.

While the embodiment illustrated in FIG. 1, shows an embodiment where one set of TAP pins 190 is externally visible from the IC boundary, the invention is not limited to this embodiment. A multi-core processor may include multiple sets of external TAP

10 pins, where the number of sets of pins is equal to or less than the number of TAPCs included in the multi-core processor. As the number of sets of external TAP pins increases, the number of possible routing configurations may also increase. The invention is not limited to a particular defined number of external TAP pins.

While TAP Core Configuration Register 135 is illustrated as being a unified

15 register, the invention is not limited to this embodiment. TAP Core Configuration Register 135 provides a variety of control functions and may, for example, be divided into smaller registers or, in another example, may be part of a larger register. In the embodiments shown, the contents of TAP Core Configuration Register 135 may be altered during TAP operation. This may allow the controlling TAPC to change during

20 operation or the TDI/TDO routing configuration to change during operation. However, other embodiments in accordance with the invention may not allow any or some of these features to be changed during operation.

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An embodiment of the invention may include a computing platform including a multi-core processor, in which the multi-core processor includes a test control mechanism, such as, in one embodiment, for example, circuit 100 in FIG. 1. In this embodiment, a computing platform may include a multi-core processor to process

5   instructions and a memory to store instructions.

An additional embodiment of the invention may comprise a technique for testing a multi-core processor, which includes providing an indicator to identify a desired testing option. This indicator may be serially shifted into and stored in a register. Based upon the testing option selected by the provided indicator, the routing of signals between a

10   plurality of test access ports (TAPs) may be dynamically arranged. The available testing options may involve, but are not limited to, routing the signals to allow the TAPs to operate in either a serial, parallel or independent fashion. In addition, there may be a testing option, which allows an error signal to be generated if the output of two or more TAPs is not equivalent or substantially equivalent. The dynamic arrangement the signal

15   routing may, but is not required to, involve only arranging the routing of signals that exist externally to the processor cores of the multi-core processor.

While certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents will now occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended

20   to cover all such modifications and changes that fall within the true spirit of the invention.

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